IN THE CLAIMS:

No claims are amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Previously Presented) An intermediate structure of a semiconductor device comprising:

at least one exposed open fuse structure on the intermediate structure of the semiconductor device; and

a metal feature on an exposed metal structure of the intermediate structure of the semiconductor device, wherein a metal of the metal feature is present on the exposed metal structure and is not present on the at least one exposed open fuse structure.

2. (Previously Presented) The intermediate structure of claim 1, wherein the metal feature comprises an electrolessly plated metal feature.

3. (Previously Presented) The intermediate structure of claim 1, wherein the metal feature is a metal layer, an interconnect cap, a redistribution layer, or a bond pad.

4. (Previously Presented) The intermediate structure of claim 1, wherein the metal feature is a metal layer.

5. (Previously Presented) The intermediate structure of claim 1, wherein the metal feature comprises a nickel, palladium, gold, tin, silver, or copper feature.

6. (Previously Presented) The intermediate structure of claim 1, wherein the metal feature comprises a nickel feature.

7. (Previously Presented) The intermediate structure of claim 1, wherein the exposed metal structure comprises at least one bond pad.

8. (Previously Presented) The intermediate structure of claim 1, wherein the intermediate structure is an intermediate structure of an SRAM or FLASH memory chip.

9-18. (Canceled)